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**PROJECT TITLE: ASSESSMENT OF THE UNIVERSAL FEASIBILITY OF USING POWER SYSTEM HARMONICS AS LOSS OF MAINS DETECTION FOR DISTRIBUTED ENERGY RESOURCES**

**CONTRACT NUMBER: RD3-21** **MILESTONE NUMBER: 11** **REPORT DATE: DECEMBER 28, 2011**

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# MILESTONE REPORT

## EXECUTIVE SUMMARY

The purpose of this project is to assess the universal applicability of harmonic signatures and/or synchrophasors as a means for detecting unintentional islanding of distributed generation equipment such as photovoltaics. This report covers the time period December 01, 2010 to December 31, 2011, and describes our progress on Milestone 11. Milestone 11 has been completed. Accomplishments in this reporting period include:

- Complete analysis of IEEE-1547 and interrelated standards. Complete report detailing recommended changes to the standards based on the foregoing work.

To meet this milestone, NPPT investigators have recommended a number of changes to IEEE 1547.8. In summary, these changes involve edits that allow future distributed generators to decouple fault detection, loss of mains detection, and overvoltage prevention. If this can be done effectively, then the 2-second maximum run-on time limit currently imposed on anti-islanding techniques could be lengthened to 5 or even 10 sec with no loss of safety or system security.

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## TECHNICAL PROGRESS

Milestone #11 consisted of:

- Complete analysis of IEEE-1547 and interrelated standards. Complete report detailing recommended changes to the standards based on the foregoing work.

The PI on this project has been actively participating in the writing of the IEEE 1547.8 standard, tentatively entitled "Draft Recommended Practice for Establishing Methods and Procedures that Provide Supplemental Support for Implementation Strategies For Expanded Use of IEEE Standard 1547". This cumbersome title attempts to convey that the mission of 1547.8 is to provide guidance as to how 1547 should be interpreted in the future as new technologies develop and new issues and situations are identified. This forward-looking focus was the reason why 1547.8 was targeted as the right part of the 1547 effort to focus on for purposes of this RDF project.

The PI carefully reviewed the entire IEEE 1547.8 draft to determine what portions of it should be modified to enable more advanced loss-of-mains detection that maintains compatibility with grid support and other future functions of distributed generators without compromising safety and system security. Most of the standard did not require modification, but we have suggested important changes to several of the key island detection provisions. In summary, the purpose of these modifications is to decouple loss of mains detection, fault detection, and temporary overvoltage protection, and the benefit of this decoupling is that it would permit lengthening of the 2-sec limit currently imposed on anti-islanding techniques.

As currently written, IEEE 1547 is a highly effective document that has proven invaluable to utilities, equipment manufacturers, and project developers. However, for a variety of reasons, it has one flaw that has persisted throughout its development. IEEE 1547 contains two tables, one in Section 4.2.3 that describes how long an inverter should operate under various abnormal voltage conditions (Table 1, reproduced from IEEE 1547 below), and another in Section 4.2.4 describing allowable operating times for abnormal frequencies (Table 2, again reproduced from the standard). Table 1 says that if the voltage drops below 50% of nominal, the distributed generator must stop energizing any portion of the area electric power system (area EPS) within 160 msec. If the voltage lies between 50% and 88% of nominal, the DG is allowed 2 sec to trip, and so forth.

**Table 1—Interconnection system response to abnormal voltages**

| Voltage range (% of base voltage[a]) | Clearing time(s)[b] |
|---|---|
| $V < 50$ | 0.16 |
| $50 \le V < 88$ | 2.00 |
| $110 < V < 120$ | 1.00 |
| $V \ge 120$ | 0.16 |

[a]Base voltages are the nominal system voltages stated in ANSI C84.1-1995, Table 1.
[b]DR ≤ 30 kW, maximum clearing times; DR > 30kW, default clearing times.

Table 2 says that for DG smaller than 30 kW, the DG must trip in 160 msec if the frequency remains outside of the range of 59.3 Hz to 60.5 Hz for that time period. If the DG is larger, a longer underfrequency trip time is allowed so that the local EPS operator can require the DG to stay online during transient underfrequency events, when DG support would be helpful to the larger system. For frequencies between 57 and 59.8 Hz, the area EPS operator can require a DG trip time of anywhere between 160 msec and 5 minutes, with the actual clearing time for any specific DG being determined by the area EPS operator on the basis of a system study or other available data. The purpose of the different levels of run-on time for different levels of low voltage or frequency is to try to allow a reasonable level of event ride-through while preventing a DG from feeding a fault.

IEEE 1547 then specifically addresses the subject of islanding in Section 4.4:

> For an unintentional island in which the DR energizes a portion of the Area EPS through the PCC, the DR interconnection system shall detect the island and cease to energize the Area EPS within two seconds of the formation of an island.

**Table 2—Interconnection system response to abnormal frequencies**

| DR size | Frequency range (Hz) | Clearing time(s)[a] |
|---|---|---|
| ≤ 30 kW | > 60.5 | 0.16 |
| | < 59.3 | 0.16 |
| > 30 kW | > 60.5 | 0.16 |
| | < {59.8 – 57.0} (adjustable set point) | Adjustable 0.16 to 300 |
| | < 57.0 | 0.16 |

[a]DR ≤ 30 kW, maximum clearing times; DR > 30 kW, default clearing times.

The problem with the standard at this point is that the reason for the 2-sec limit mentioned in Section 4.4 of the Standard was because the committee was and is mixing fault detection and island detection concerns in a way that does not satisfactorily address either. The condition under which an unintentional island may run on longer than 2 sec is one in which the potential island has an extremely close match between the real and reactive power being generated by sources inside the island, and the real and reactive power consumption of all loads and losses in the island. If the real powers are mismatched, then for inverter-based DG the voltage will collapse; if the reactive powers are mismatched, then again for inverter-based DG the frequency will deviate from nominal. Thus, in any mismatched case, the DG can detect the island on the basis of abnormal voltage or frequency.

If there is a close match between generation and load, then this is the circumstance in which specialized "anti-islanding" or loss-of-mains detection techniques are designed to act. This includes all active anti-islanding as well as the passive and communications-based methods studied in this RDF project: they are designed to cover the case of an island being formed under a very close generation-load matching condition.

Many 1547 committee members have been suggesting shortening the 2-sec limit because of the risk of asynchronous reclosure during a fault. In fact, some have suggested shortening it to as little as 6 cycles because of the possibility that a utility may be using very fast reclosure. However, if there is a fault, it is virtually impossible to obtain a generation-load match because the fault will demand far more power than the DG can supply. This is especially true for inverter-based DG, but it applies for rotating machines as well. The very low fault impedance will appear to the DG as an extremely large load that is larger than the DG's capacity, and an undervoltage condition will result. There will also be abnormal sequence components, if the fault is asymmetrical; changes in line-line phase relationships, for line-line faults; and recognizable changes in harmonic spectra, among other abnormalities in endpoint voltages. If the island does contain a fault, then very fast DG action is required, both to avoid feeding the fault and to avert an asynchronous reclosure. However, the foregoing discussion makes two key points clear: 1) if there is a fault, ***there are several techniques other than anti-islanding that could be used much more effectively to detect the fault***; and 2) existing anti-islanding, since it is designed to cover a matched generation-load case, is not designed for fault detection. In other words, ***existing anti-islanding is designed to detect non-faulted islands, and is NOT designed to detect faults***.

This is where the flaw in IEEE 1547 becomes apparent. Anti-islanding is designed to detect a non-faulted, generation-load matched case, but 1547 does not make this distinction. A better solution would be to allow DG to have dedicated island, fault, and overvoltage prevention means. A non-faulted island case could occur during a source switchover, or other similar feeder reconfiguration event. In that case, the 2-sec limit is far shorter than is really needed to provide adequate protection. Some utilities have suggested that 5 sec would be adequate; others have suggested 10 sec in this case. However, it is clear that there is no reason why the island must be detected in 2 sec. The quandary is now apparent: some desire to see the 2-sec limit shortened because they are concerned about faults, but others want to see it lengthened because the case actually covered by anti-islanding methods should not require a trip in 2 sec, and both groups are right.

To solve this problem, the improvement in IEEE 1547 that we are suggesting is to write sections into 1547.8 that allow for longer than 2 sec for loss of mains detection, ***if the DG has the capability to reliably detect faults and overvoltages using means other than the anti-islanding controls***. In other words, in the future, if DG (particularly larger, 3-phase DG) have effective built-in fault detection and overvoltage protection, then there is no safety or protection-based reason why IEEE 1547 could not allow for longer than 2 sec to detect an island with matched generation and loads.

The reason why this is an improvement from the perspective of this RDF project is that there exist a number of passive island detection methods that can be as effective as any active method if a) they are allowed longer than 2 sec to detect a power-matched island, and b) they are not inappropriately applied to fault detection. This future capability to decouple fault detection, overvoltage prevention, and loss of mains detection would enable the use of a range of new and innovative techniques to prevent unintentional islands while facilitating grid support functions, all without compromising system security or safety.

To implement this, the PI on this project has submitted to the IEEE 1547.8 committee an extensive list of edits designed to address the concerns discussed above, and allow the standard to recognize a separation of island, fault and overvoltage detection in distributed generators. These comments have been discussed by the 1547.8 committee on a conference call that took place in early December 2011, and will be thoroughly debated and edited by the entire 1547.8 committee during a meeting to be held in early February 2012.

## NEXT STEPS

Our Milestone #12 involves attendance at three or more IEEE 1547.8 meetings. The PI has already attended two 1547.8 meetings in person and one via conference call, and plans to attend a third in-person meeting in Atlanta in February 2012. Thus, this milestone will be completed by the end of February 2012.

## PROJECT STATUS

We are on track to submit Milestone Report #12 by the end of February 2012.

## LEGAL NOTICE